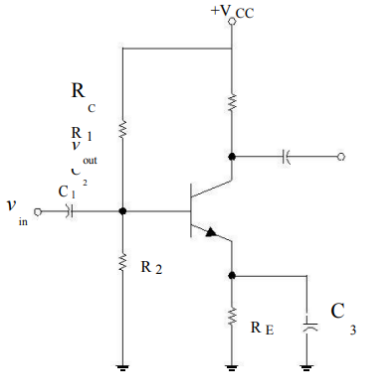
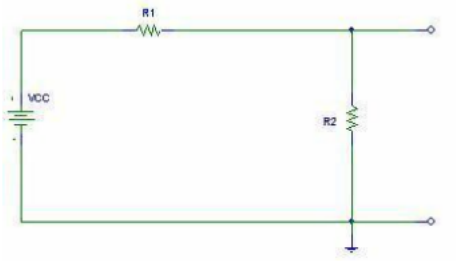
Voltage divider bias



This is the biasing circuit wherein, ICQ and VCEQ are almost independent of β. The level of IBQ will change with β so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point. Two methods of analyzing a voltage divider bias circuit are: Exact method – can be applied to any voltage divider circuit Approximate method – direct method, saves time and energy, can be applied in most of the circuits. Exact method In this method, the Thevenin equivalent network for the network to the left of the base terminal to be found.

To find Eth



From the above circuit,

$$E_{th} = V_{R2} = R_2 V_{CC} / (R1 + R2)$$

In the above network, applying KVL

$$(E_{th} - V_{BE}) = I_B [R_{th} +(\beta + 1) R_E]$$

$$I_B = (E_{th} - V_{BE}) / [R_{th} +(\beta + 1) R_E]$$

Analysis of Output loop KVL to the output loop:

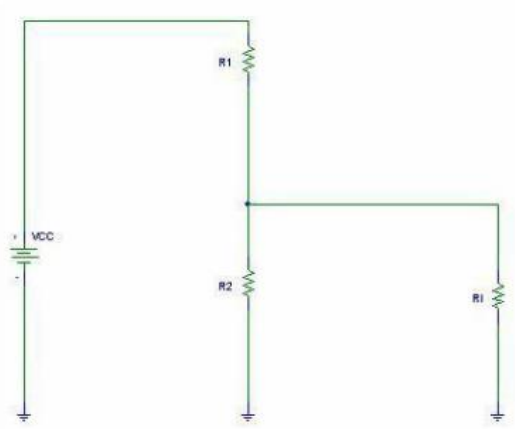
VCC = ICRC + VCE + IERE IE ≅ IC Thus, VCE = VCC – IC (RC + RE)

Note that this is similar to emitter bias circuit.

Approximate analysis:

The input section of the voltage divider configuration can be represented by the network shown in the next slide.

Input Network



The emitter resistance RE is seen as (β+1)RE at the input loop. If this resistance is much higher compared to R2, then the current IB is much smaller than I2 through R2.

This means, Ri >> R2 OR (β+1)RE ≥ 10R2 OR βRE ≥ 10R2 This makes IB to be negligible. Thus I1 through R1 is almost same as the current I2 through R2. Thus R1 and R2 can be considered as in series. Voltage divider can be applied to find the voltage across R2 (VB) VB = VCCR2 / (R1 + R2)

Once VB is determined, VE is calculated as, VE = VB – VBE After finding VE, IE is calculated as, IE = VE / RE IE ≅ IC VCE = VCC – IC (RC + RE