Unit 2: Silicon Controlled Rectifier (SCR)

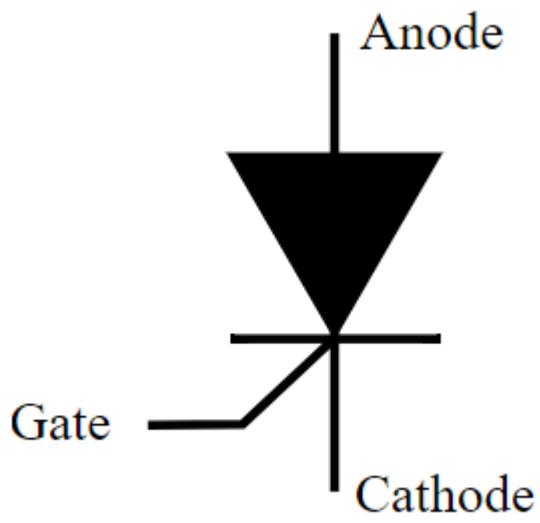
Module 3: Structure, Principle of operation, V-I characteristics and Two-transistor model of SCR.

Introduction:

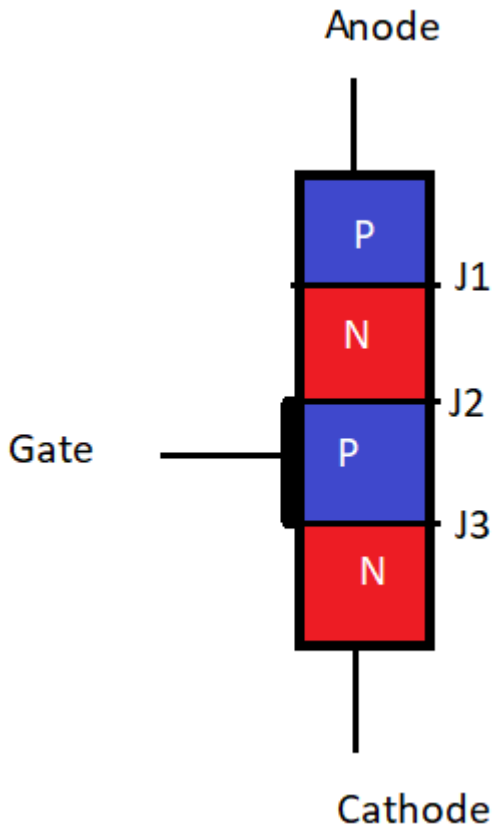
A silicon-controlled rectifier is a four-layer solid-state current-controlling device. The name "silicon-controlled rectifier" is General Electric's trade name for a type of thyristor.

SCRs are mainly used in electronic devices that require control of high voltage and power. This makes them applicable in medium and high AC power operations such as motor control function.

An SCR conducts when a gate pulse is applied to it, just like a diode. It has four layers of semiconductors that form two structures namely; NPNP or PNPN. In addition, it has three junctions labeled as J1, J2 and J3 and three terminals anode, cathode and a gate. An SCR is diagrammatically represented as shown below.



The anode connects to the P-type, cathode to the N-type and the gate to the P-type as shown below.



Principle of Operation

The Principle of operation of SCR can be explained using the Modes of Operation in SCR

OFF state forward blocking mode − Here the anode is assigned a positive voltage, the gate is assigned a zero-voltage disconnected and the cathode is assigned a negative voltage. As a result, Junctions J1 and J3 are in forward bias while J2 is in reverse bias. J2 reaches its breakdown avalanche value and starts to conduct. Below this value, the resistance of J1 is significantly high and is thus said to be in the off state.

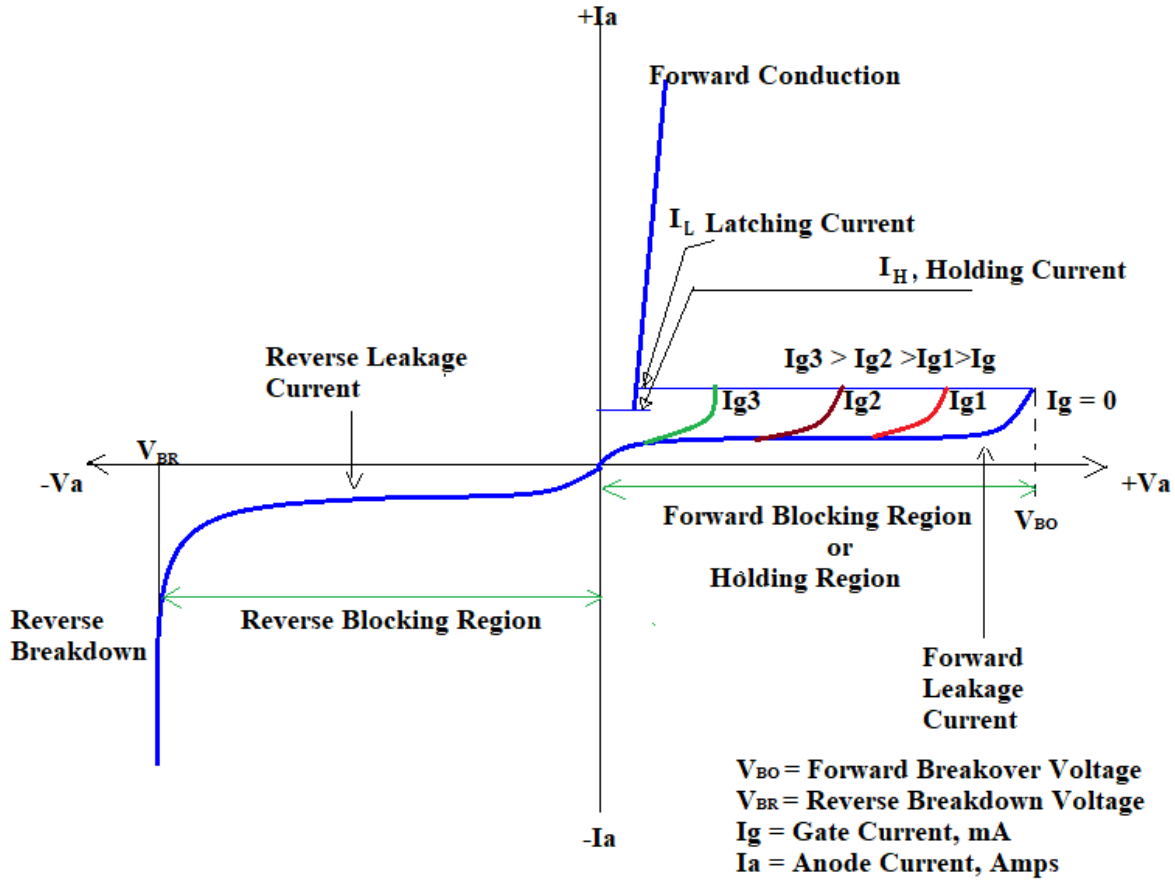
ON state conducting mode − An SCR is brought to this state either by increasing the potential difference between the anode and cathode above the avalanche voltage or by applying a positive signal at the gate. Immediately the SCR starts to conduct, gate voltage is no longer needed to maintain the ON state

Reverse blocking mode (J1 and J3 reverse biased and J2 forward biased).

This compensates the drop in forward voltage. This is due to the fact that a low doped region in P1 is needed. It is important to note that the voltage ratings of forward and reverse blocking are equal. The SCR does not conduct in this mode

Reverse Breakdown Mode: Avalanche Breakdown. This is not a safe operation.

V-I Characteristics of SCR



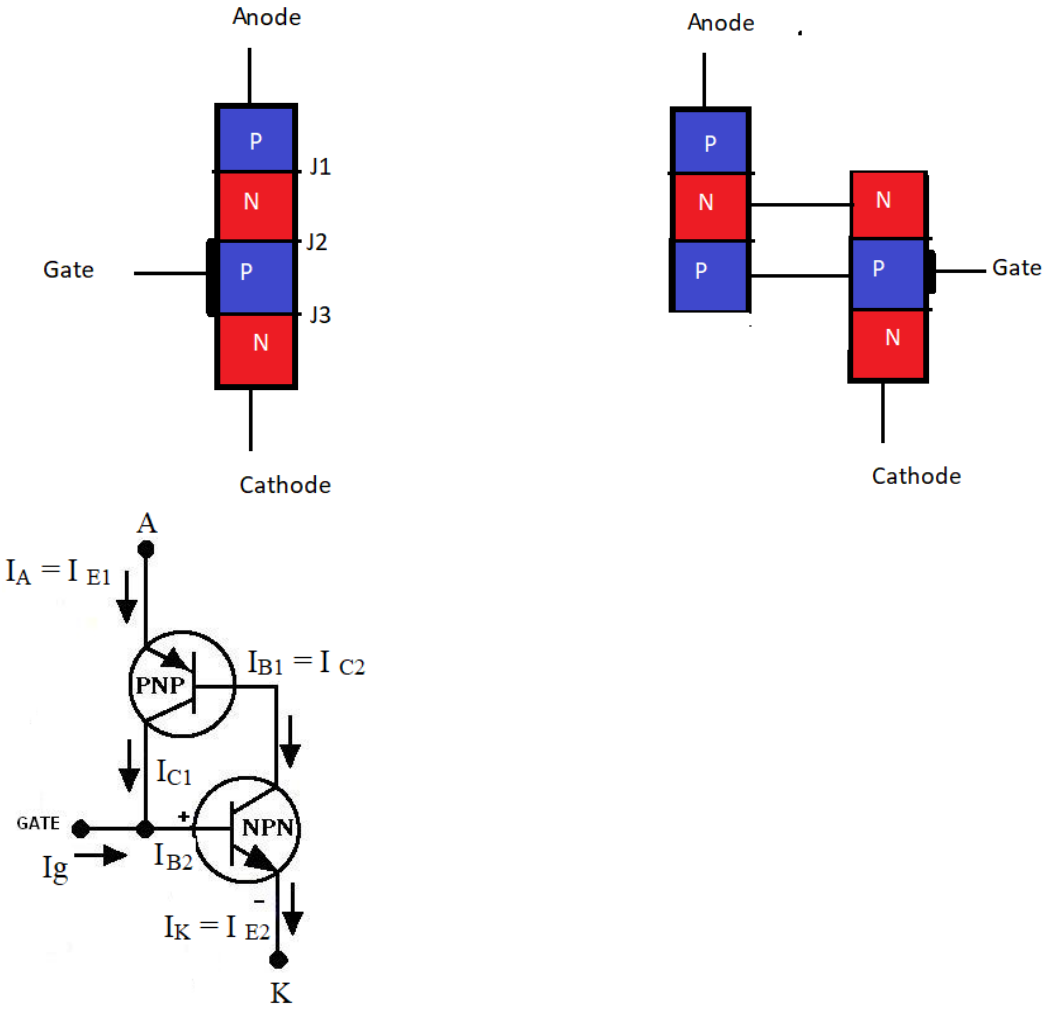
Latching Current:

The latching current of an SCR specifies a value of the anode current slightly higher than the holding current which is the minimum value required to sustain conduction immediately after the SCR is switched from the OFF state to the ON state and the gate signal is removed. Once the latching current is reached, the SCR remains in the ON state until the anode current is decreased below the holding current value.

Holding Current:

It is the minimum value of the anode current, necessary in the anode circuit to keep the SCR conducting (with gate open).

Two Transistor Analogy of SCR



Here, I_C is collector current, I_E is emitter current, I_{CBO} is forward leakage current, α is common base forward current gain and relationship between I_C and I_B is

$$I_C = \beta I_B$$

Where, I_B is base current and β is common emitter forward current gain.
Let's for transistor T_1 this relation holds

$$I_{C1} = \alpha_1 I_a + I_{CBO1} \ldots\ldots (i)$$

And that for transistor T_2

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \ldots\ldots (ii)\ again\ I_{C2} = \beta_2 I_{B2}$$

Now, by the analysis of two transistors model we can get anode current,

$$I_a = I_{C1} + I_{C2}\ \ [applying\ KCL]$$

From equation (i) and (ii), we get,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \ldots . (iii)$$

If applied gate current is I_g then cathode current will be the summation of anode current and gate current i.e.

$$I_k = I_a + I_g$$

By substituting this valyue of I_k in (iii) we get,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$
$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

From this relation we can assure that with increasing the value of

$(\alpha_1 + \alpha_2)$ towards unity, corresponding anode current will increase. Now the question is how $(\alpha_1 + \alpha_2)$ is increasing? Here is the explanation using **two transistor model of SCR**.
At the first stage when we apply a gate current I_g, it acts as base current of T_2 transistor i.e., $I_{B2} = I_g$ and emitter current of the T_2 transistor $I_{E2} = I_k$. Hence establishment of the emitter current gives rise α_2 as

$$\alpha_2 = \frac{I_{CBO1}}{I_g}$$

Presence of base current will generate collector current as

$$I_{C2} = \beta_2 \times I_{B2} = \beta_2 I_g$$

This I_{C2} is nothing but base current I_{B1} of transistor T_1, which will cause the flow of collector current,

$$I_{C2} = \beta_1 \times I_{B1} = \beta_1 \beta_2 I_g$$

I_{C1} and I_{B1} lead to increase I_{C1} as $I_a = I_{C1} + I_{B1}$

and hence, α_1 increases. Now, new base current of T_2 is $I_g + I_{C1} = (1 + \beta_1 \beta_2) I_g$

, which will lead to increase emitter current $I_k = I_a + I_{C1}$

and as a result α_2 also increases and this further increases

$$I_{C2} = \beta_2 (1 + \beta_1 \beta_2) I_g$$

As $I_{B1} = I_{C2}$, α_1 again increases. This continuous positive feedback effect increases $(\alpha_1 + \alpha_2)$ towards unity and anode current tends to flow at a very large value.

The value current then can only be controlled by external resistance of the circuit.