Welcome students.

Today's session for program Bachelor of Science

Subject computer science semester.

4 Course Code CSC 104 Course title

computer organization and operating system.

Title of the unit.

Basic computer organization and design.

Module name.

RISC CISC architecture module number 14,

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Today's session outline will discuss

RISC Architectures
What is RISC?
RISC Architecture
Characteristic of RISC
Advantages of RISC Architecture
Disadvantages of RISC Architecture
Examples of RISC processors

CISC Architectures
What is CISC?
CISC Architecture
Characteristic of CISC
Advantages of CISC Architecture
Disadvantages of CISC Architecture
Examples of CISC processors

At the end of this module ,the learner will be able to:

Describe RISC Architecture

Describe CSC Architecture

Differentiate between RISC and CISC Architectures.

What is risk?

The RISC is a Reduced Instruction Set Computer microprocessor, and its architecture includes a set of instructions that are highly customized.

A reduced instruction set computer is a computer that only uses simple commands that can be divided into several instructions that achieve low-level operation within a single CLK cycle, as its name proposes “Reduced Instruction Set”.

The main function of this is to reduce the time of instruction execution by limiting as well as optimizing the number of commands. So each command cycle uses a single clock cycle where every clock cycle includes three parameters namely fetch, decode & execute.

The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating and storing operations just like a load command will load data, store command will store the data.
The kind of processor is mainly used to execute several difficult commands by merging them into simpler ones.

RISC processor needs a number of transistors to design and it reduces the instruction time for execution.

RISC Architecture
It is a CPU design plan based on simple orders and acts fast.

This is a small or reduced set of instructions. Here, every instruction is expected to attain very small jobs.

In this machine, the instruction sets are modest and simple, which help in comprising more complex commands.

Each instruction is of a similar length; these are wound together to get compound tasks done in a single operation.

Most commands are completed in one machine cycle. This pipelining is a crucial technique used to speed up RISC machines.

Now we will discuss RISC Processor Block Diagram

RISC processor is implemented using the hardwired control unit. The hardwired control unit produces control signals which regulate the working of processors hardware. RISC architecture emphasizes on using the registers rather than memory.
This is because the registers are the ‘fastest’ available memory source. The registers are physically small and are placed on the same chip where the ALU and the control unit are placed on the processor.
The RISC instructions operate on the operands present in processor’s registers.

we don’t have the “microprogram control store” or the “control memory” like in the CISC architecture .

It is just because all instructions in RISC are simple and execute one instruction per cycle.

So, here the instructions are hardwired and there is no need for control store. For each operation, we will have as defined hardwire. Making an instruction hardwired is making a function or operation in instruction permanent using connected circuits.

RISC Characteristics

Simpler instruction, hence simple instruction decoding.
Instruction come under size of one word.
Instruction take single clock cycle to get executed.
More number of general purpose register.
Simple Addressing Modes.
Less Data types.
Pipeline can be achieved.

RISC Advantages
The performance of RISC processors is often two to four times than that of CISC processors because of simplified instruction set.

This architecture uses less chip space due to reduced instruction set. This makes to place extra functions like floating point arithmetic units or memory management units on the same chip.

The per-chip cost is reduced by this architecture that uses smaller chips consisting of more components on a single silicon wafer.

RISC processors can be designed more quickly than CISC processors due to its simple architecture.

The execution of instructions in RISC processors is high due to the use of many registers for holding and passing the instructions as compared to CISC processors.

RISC Disadvantages

The performance of a RISC processor depends on the code that is being executed. The processor spends much time waiting for first instruction result before it proceeds with next subsequent instruction, when a compiler makes a poor job of scheduling instruction execution.

RISC processors require very fast memory systems to feed various instructions. Typically, a large memory cache is provided on the chip in most RISC based systems.

RISC instruction size is reduced but more instructions are required to perform an operation when compared with CISC. So, we can say that the length of the program is increased.

The machine instructions are hardwired in RISC so, it would cost if any instruction needs modification.

It finds is difficulty in processing complex instruction and complex addressing mode.

RISC instructions do not allow direct memory to memory transfer, it requires Load and Store instructions to do so.

RISC Examples

MIPS
SPARC
IBM POWER instruction set
Alpha
RISC-V
ARM architecture.

What is CISC ?
It was developed by the Intel Corporation and it is Complex Instruction Set Computer.

This processor includes a huge collection of simple to complex instructions. These instructions are specified in the level of assembly language level and the execution of these instructions takes more time.

A complex instruction set computer is a computer where single instructions can perform numerous low-level operations like a load from memory, an arithmetic operation, and a memory store or are accomplished by multi-step processes or addressing modes in single instructions, as its name proposes “Complex Instruction Set ”.

This processor moves to decrease the number of instructions on every program & ignore the number of cycles for each instruction.

It highlights to assemble complex instructions openly within the hardware as the hardware is always as compared with software. However, CISC chips are relatively slower as compared to RISC chips but utilize small instruction as compare with RISC.

The main idea is that a single instruction will do all loading, evaluating and storing operations just like a multiplication command will do stuff like loading data, evaluating and storing it, hence it's complex.

CISC Architecture
The main objective of a CISC processor is to minimize the program size by reducing the number of instructions in a program. This is done by 'embedding some of the low-level instructions in a single complex instruction'. Later when decoded this instruction generates several microinstructions to execute.

Now if a program/software is getting simplified then the hardware has to get on work and must be able to perform the complex tasks. That's why a CISC processor has complex hardware.

Now we will discuss CISC Processor Block Diagram

Here, you have a special microprogram control unit that uses a series of microinstructions of the microprogram stored in the "control memory" of the microprogram control unit and generate the control signals.

The control units access the control signals produced by the microprogram control unit & operate the functioning of processors hardware.

Instruction and data path fetches the opcode and operands of the instructions from the memory.
Cache and main memory is the location where the program instructions and operands are stored.

CISC Characteristics
Complex instruction, hence complex instruction decoding.
Instruction are larger than one word size.
Instruction may take more than single clock cycle to get executed.
Less number of general purpose register normally from 5 to 20 as operation get performed in memory itself.
Complex Addressing Modes.
More Data types.
The code length is very short, so it needs extremely small RAM.
It highlights the instruction on hardware while designing as it is faster to design than the software.
It gives simple programming within assembly language.

CISC Advantages

Microprogramming is easy to implement and much less expensive than hard wiring a control unit.

It is easy to add new commands into the chip without changing the structure of the instruction set as the architecture uses general-purpose hardware to carry out commands.

This architecture makes the efficient use of main memory since the complexity (or more capability) of instruction allows to use less number of instructions to achieve a given task.

The compiler need not be very complicated, as the micro program instruction sets can be written to match the constructs of high level languages.

CISC Disadvantages

A new or succeeding versions of CISC processors consists early generation processors in their subsets (succeeding version). Therefore, chip hardware and instruction set became complex with each generation of the processor.

The overall performance of the machine is reduced because of slower clock speed.

The pipeline execution within the CISC will make it difficult to use.

The performance of this processor may change based on the executed code because the next commands may depend on the earlier instruction for their implementation within a cycle.

These processors need very quick memory to keep different instructions that use a huge collection of cache memory to react to the command within less time.

CISC Examples

IBM 370/168
VAX 11/780
Intel 386, 486
Pentium, Pentium Pro, Pentium II, Pentium III
Motorola’s 68000, 68020, 68040, etc.

Conclusion

There is no better architecture.
When microprocessors and microcontroller were first being introduced, they were mostly CISC mainly because of the lack of software support for RISC.
Later a few companies started delving into the RISC architecture such as Apple.

The CISC architecture was becoming difficult to improve and develop. Intel however had a lot of resources and were able to overcome most of the major roadblocks. They were doing this mainly to make all their hardware and software back compatible with their initial 8086 processors.

Currently, the boundary between RISC and CISC architectures are very blurred as both hardware and software support for RISC and CISC are readily available.

These are the references.

Thank you.