Welcome students, semester four, course.title is computer organization and operating systems,module number is 17 and module name is programmed IO interrupt driven IO and direct memory access.

In this lecture we will learn about programmed IO, interrupt driven IO and direct memory access.

At the end of the lecture,student will be able to explain the programmed IO method of data transfer,Explain the interrupt drivenIO method of data transfer.
Explain the concept of direct memory access.Define the DMA burst. Define cycle stealing.

To begin with,we have programmed IO in this method Operations are the result of IO instructions written in the computer program.
Each data transfer is initiated by an instruction in the program.
The transfer is from CPU resistor to peripheral devices or vice versa.

Once the data transfer is initiated,the CPU is required to monitor the interface to see when the transfer can be made.
It is up to the programmed instructions executed in the CPU to keep close tabs on everything that is taking place in the interface unit and the IO device.
In this technique,CPU is responsible for executing data from the memory for output and storing data in memory for executing of programmed IO.

The execution process is shown in this flow chart. First, CPU will issue the read or write command to IO module.
After issuing the command I/O module will inform about its status to CPU.
If status is ready than CPU reads word from IO module and write it to memory(vice-versa) .
If status is busy than CPU will issue again a new command. After getting a command, I/O module will inform about his status to CPU.If status is ready again then it can execute the Instruction.
After executing it will check if transfer is complete if transfer is complete then it will execute next instruction.

There is a drawback of programmed IO.
It is a time consuming process as a lot of CPU time is wasted.

Next, we have interrupt initiated IO in interrupt initiated IO method an interrupt facility is used to inform the device about the start and end of transfer.
When the interface determines that the device is ready for data transfer, it generates an interrupt request and sends it to the computer.
When the CPU receives such a signal,It temporarily stops the execution of program and branches to a service program to process the IO transfer, and after completing it returns back to the task, what it was originally performing.

This is a flow chart for the execution process of interrupt initiated IO.CPU issues the read or write command to IO module.After getting the command,
IO module informs about its status to CPU.
If status is ready then it will execute execute the instruction,i. e. it will read word from IO module and it will write it to memory(vice versa).
After transfer is complete,it will check the status.if status is ready then it will execute next instruction.

Otherwise it will issue another command.
It will check again if IO module is free and it will continue the process of the execution.

Next is Direct memory access in direct memory access the interface transfers the
data into and out of the memory unit through the memory bus.
Removing this CPU from the path and letting the peripheral device manage the memory buses directly would improve the speed of the transfer. and this technique is called as direct memory access.

During the DMA transfer, the CPU is idle and has no control of the memory buses.
The DMA controller takes over the buses to manage the transfer directly between IO devices and memory.

The CPU may be placed in an idle state. in a variety of ways.
By using a special control signals like Bus requests (BR) and Bus grant(BG).
These two control signals in the CPU are used to transfer data.
The bus request input is used bythe DMA controller to request the CPU.When this input is active,the CPU terminates the execution of the current instruction and places the address bus, data bus and read write lines into a high impedance state.

High impedance state means that
the output is disconnected.

Here in the block diagram
we have Burst request Signal, Bus grant, signal, address bus, data bus, read and write signal.

The CPU activates the bus grant output, which informs the external DMA to conduct memory transfer without processor using bus request.
When the DMA terminates the transfer,It disables the bus request line.The CPU disables the bus grant, takes control of the buses and return to its normal operation.

Transfer can be made in several ways.One way is using DMA burst.And the another way is cycle stealing.

In the DMA Burst,
transfer a block sequence consisting of a number of memory words is transferred in continuous burst while the DMA controller is master of the memory buses.

In Cycle stealing process.DMA controller transfer one data word at a time after which it must return control of the buses to the CPU.

DMA controller needs the usual circuits of an interface to communicate with the CPU and IO device.
DMA Controller plays major role while transferring the data between IO devices and memory.
In DMA controller.We are having three major registers those are address register, word countregister and control register.

Address register contains an address to specify the desired location in memory.

Word count Register holds the number of words to be transferred.The resistor is incremented ordecremented by one after each word transfer is complete.

Control register specifies the mode of transfer.

The unit communicates with the CPU, via the data bus and control lines.The registers in the DMA are selected by the
CPU through the address bus by enabling DMA select and register select inputs. The read and write inputs are Bidirectional.

When the bus grant input is 0,the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA registers.

When Bus Grant is equal to 1 the DMA can communicate directly with the memory by specifying an address in the address bus and activating the read or write control.

This is a block diagram of DMA controller Wherein we are having the DMA controller
with all the registers like address register, word count register, control register at the same time we're having the signals DMA select, register select and read and write Bidirectional signals.DMA request and burst grant are the two signals used to take control from the CPU.

The CPU communicates with the DMA through the address and data buses as with any interface unit.
The DMA has its own address which activates the DMA Select and register select lines.
The CPU initializes the DMA through the data bus.
Once the DMA receives the start control command,it can transfer between peripheral and the memory.

When BG is set to 0 the read and write are input lines allowing the CPU to communicate with the internal DMA registers.
When BG is set to 1 the read and write are output lines from the DMA controller to the random access memory to specify read or write operation of data.

They said my references.

Thank you.