Course title is microcontroller Architecture and Programming.

Name of the module is “Memories”

Outline of the course:

a) Internal ROM
b) Internal RAM
c) Special Function Registers

Learning Outcomes of the course:

At the end of the module, learner will be able to:

Understand the different memory of the 8051 microcontroller and their functions.

Let us revise the unique features of 8051.

Dear students!

In previous module, we have learned about the different hardware aspects of 8051microcontroller. Let us revise the unique features of 8051. And are shown in table 1

1. On chip ROM of 4KBytes ,
2. Internal RAM, 128 bytes
3. 2 number of Timers,
4. 32 I/O Pins ,
5. One serial Port, and
6. 6 Interrupt Sources

With these basic features, the 8051-microcontroller can be made to control the operation, of any simple or fairy complex digital control application.

Internal Memory

A computing machine, must have memory, for program code bytes (i.e. instructions) in ROM, and RAM memory, storage of variable data that can be altered as the program runs. The 8051 has internal ROM and RAM memory for these functions. And special memory, called Special Function register (SFR).

Additional memory, can be added externally, using suitable circuits.

a) **Internal ROM:** as per the feature, the 8051 has 4 Kilo bytes space to store the instructions OR Program code bytes, to run the machine. This is built-in ROM, which occupies the address space from 0000h to 0FFFh.

The Program counter in general, is used to address the program code bytes from 0000h to FFFFh, for 16 bit addressing system. The program addresses higher than 0FFFh, which exceeds the internal ROM capacity, will cause the 8051 to automatically, fetch the code bytes, from external program memory. The codes bytes can also be fetched exclusively, from an external memory addresses 0000h to FFFFh, by connecting the external access (EA),

pin 31 on the chip , to ground. The program counter PC does not care, where the code is. Therefore the circuit designer should decide whether the code is found in internal memory, totally in external memory or in combination of both.

b) Internal RAM: the 8051, consists of 128 bytes, of internal RAM for temporary storage and is organised into three distinct areas:

1. Thirty-two bytes from address 00h to 1Fh that make up 32 working registers, organized as four BANKS of eight- registers each. The four register banks are numbered 0 to 3 and are made up of eight registers named R0 to R7. Each register can be addressed by name (when its bank is selected) or by its RAM address.

Example. R0 of bank 3 is, **R0** (if bank 3 is currently selected) or address **18h** (whether bank 3 is selected or not).

CY	AC	F0	RS1	RS0	OV	-	P

Bits **RS0** and **RS1** in the PSW register, determine which bank of registers is currently in use at any time when the program is running. Register banks not selected, can be used as general-purpose RAM.

RS1	RS2	Selection
0	0	Register Bank 0
0	1	Register Bank 1
1	0	Register Bank 2
1	1	Register Bank 3

Bank 0 is selected on reset.

2. A bit-addressable area of 16 bytes occupies, RAM byte addresses 20h to 2Fh, forming a total of 128 addressable bits.

An addressable bit, may be specified by its bit address of 00h to 7Fh, or 8 bits may form any byte address from 20h to 2Fh. Thus, for example, bit address 4Fh is also bit 7 of byte address 29h.

Addressable bits are useful when the program need only to remember a binary event (like Fan switch is “ON”, light switch to “OFF”, etc.) i.e. Individual event can be controlled.

This is what a microcontroller is different from microprocessor.

3. A general-purpose RAM area above the bit area, from 30h to 7Fh, is addressable as bytes.

C) Special Function Registers (SFR)

The 8051 consists of 128-byte of internal RAM, having an addresses from 00h to 7Fh. Beyond 7Fh address, there is a group of specific internal registers, each called a Special-Function

register (SFR), which may be addressed much like internal RAM, using addresses from 80h to FFh.

The SFR names, and equivalent internal RAM addresses are shown in Table.

Some SFRs in table, which are highlighted in yellow colour, are also bit addressable, like the bit area of internal 128 bytes RAM. This feature allows the programmer to change only what needs to be altered, leaving the remaining bits in that SFR unchanged.

Not all of the addresses from 80h to FFh are used for SFRs, and attempting to use an address that is not defined, will give unpredictable results.

Note that, the Program Counter is not part of the SFR and has no internal RAM address.

SFR's are named in certain *opcodes* by their functional names, such as A or B or PSW and are also referenced by other *opcodes* by their addresses, such as 0E0h or 0F0h or 0D0h.

Note that, any address used in the program must start with a number; thus address E0h for the A- SFR begins with 0. Failure to use this number - convention, will result in an assembler error when the program is assembled.

1) A and B - CPU Registers

The 8051 contains **34** general-purpose, or working-registers. Two of these, are- registers A and B, which hold the results of many instructions, particularly math and logical operations, of the 8051 central processing unit (CPU).

The other 32, registers are arranged as part of internal RAM in four banks, B0 - B3, of eight registers. (4X 8bit).

The A (accumulator) register, is the most versatile of the two CPU registers and is used for many operations, including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The A register is also used for all data transfers between the 8051 and any external memory. The B register is used with the A register for multiplication and division operations

and has no other function, other than as a location where data may be stored.

2) Data Pointer

The **DPTR** register is made up of TWO 8-bit registers, named DPH and DPL, which are used to furnish memory addresses, for internal and external code, access and external data access. The DPTR is under the control of program instructions and can be specified by its 16-bit name, DPTR, or by each individual byte

name, DPH and DPL. DPTR does not have a single internal address; DPH and DPL, each, has assigned address.
Sr. Number 12 of the SFR table is, Program Status Word.

3) Flags and the Program Status Word (PSW)

Flags are 1-bit registers provided, to store the results of certain program instructions. Other instructions, can test the condition of the flags and make decisions based on the flag states. In order that the flags may be conveniently addressed, they are grouped inside the program status word (PSW) and the power control (PCON) registers.

The 8051 has four math flags, that respond automatically to the outcomes of math operations and three general-purpose user flags that can be set to “1” or cleared to “0” by the programmer as desired. The math flags include Carry (C), Auxiliary Carry (AC), Overflow (OV), and Parity (P). Note that all of the flags can be set and cleared by the programmer at his will. The math flags, however, are also affected by math operations.

The PSW contains the math flags, user program flag F0, and the register select bits RS1 & RS2 that identify which of the four general-purpose register banks, is currently in use by the program.
Sr. No. 15 is, Stack Pointer SFR register.

4) The Stack and the Stack Pointer

The stack refers to an area of internal RAM that is used in conjunction with certain opcodes to store and retrieve data quickly. The 8-bit Stack Pointer (SP) register is used by the 8051, to hold an internal RAM address that is called the ***top of the stack***. The address held in the SP register is the location in internal RAM, where the last byte of data was stored by a stack operation.

When data is to be placed on the stack, the SP increments before storing data on the stack, so that the stack grows up as data is stored. As data is retrieved from the stack, the byte is read from the stack, and then the SP decrements to point to the next available byte of stored data.

The SP is set to 07h, when the 8051 is reset and can be changed to any internal RAM address by the programmer.

The stack is limited in height to the size of the internal RAM. The stack has the potential (if the programmer is not careful to limit its growth) to overwrite valuable data in the register banks, bit - addressable RAM, and scratch-pad RAM areas. The programmer is responsible for making sure the stack does not grow beyond predefined bounds.

The stack is normally placed high in internal RAM, by an appropriate choice of the number(address) placed in the SP

register, to avoid conflict with the register bank, bit address register, and scratch-pad internal RAM areas.

5) Program Counter and Data Pointer

The 8051 contains two 16-bit registers: the program counter (PC) and the data pointer (DPTR). Each is used to hold the address of a byte in memory.

Program instruction bytes, are fetched from locations, in ROM that are addressed by the PC. Program ROM may be on the chip at addresses 0000h to 0FFFh, external to the chip for addresses that exceed 0FFFh, or totally external for all addresses from 0000h to FFFFh. The PC is automatically incremented after every instruction byte is fetched, and may also be altered by certain instructions. The PC is the only register that does not have an internal address.

Remaining SFR’s will be covered in next the topic as and when required.

These are the reference/ books used for this module.

Thank you very much.