

Title of the paper is, Microcontroller Architecture and Programming.
Name of the module is “Counters and Timers.”

Outline of the Course is:

1. Introduction
2. Timers
3. Counters

Learning Outcomes of the course is:

At the end of the module, learner will be able to:
Describe the various operating modes of the timer & counters and associated control registers.

Dear students!

In the last module we have learned about the different special function registers of 8051.

To list few are A, B, SP, PC, DP, PSW etc. These registers play a very important role in control applications.

A is very important register of microcontroller,
B is used for Maths operations,
PSW register contains flags etc.

In the current module we are going to learn about the SFR at Sr. No. 16, 17,.... 21 of the table seen on the screen and are used for counting and time keeping.

Counters and Timers:

Many microcontroller applications require the counting of external events, such as the frequency of a pulse train, or the generation of

precise internal time delays between the computer actions. Both of these tasks, can be accomplished using software techniques; but the software loops used for counting or timing, keeps the processor occupied so that other, perhaps more important, functions cannot be done.

To relieve the processor of this burden, two 16-bit up counters, named **T0** and **T1**, are provided for the general use of the programmer. Each counter may be programmed to count internal clock pulses, acting as a **timer**, or programmed to count external pulses as a **counter**.

Let me make clear, the difference between the Timer & Counter. The counter, counts the internal clock pulses derived from the crystal while timer counts the pulses supplied to it externally from the source like signal generator. Otherwise they both do the same function.

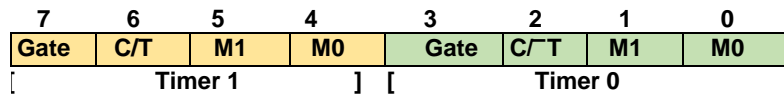
The counters are divided into two, 8-bit registers called the timer low (TL0, TL1) and high (TH0, TH1) bytes. This is seen in the table: SFR 18,19,20 & 21.

All counter action is controlled by:

- i) bit states in the timer mode control register (TMOD), {Sr. No.16}
- ii) the timer/counter control register (TCON), {Sr. No.17}, and
- iii) certain program instructions; to be done by the programmer.

The Timer Mode Control (TMOD) Special Function Register

TMOD Register is dedicated solely to the two timers and can be considered to be two duplicate 4-bit registers, each of which controls the action of one of the timers.



1. Bit 7 OR bit 3, of TMOD register is called the GATE and is a control bit. This has a function to RUN OR STOP timer 1/0; accordingly, the programmer has to write 1 OR "0" in this location.
2. Bit 6 OR 2, is a control to make counter to count the internal clock pulses (Timer) OR External pulses (Counters).
When it is set to "1" by programmer , timer 1/0 act as a counter by counting pulses from external input pins 3.5 (T1) or 3.4 (T0) of the chip. OR when changed by programmer to "0", acts timer by counting internal frequency clock.
3. Bit 5/1 and 4/0 are the control bits together, decides the mode of operation of timer OR counter as per the table 1 shown on the display.

M1	M0	Timer Mode
0	0	0
0	1	1
1	0	2
1	1	3

Note that, the TMOD register is not bit addressable. The programmer need to write a full 8 bit byte in this register every time to change the function.

TCON Register:



TCON Register is a SFR, that has control bits and flags for the timers, in the upper nibble (i.e. first 4 bits). And control bits and flags for the external interrupts in the lower nibble. In this module we are concentrating on the Counter & Timer, only. Therefore, will not focus on the lower nibble.

Let us see the bits assigned to TCON register.

1. Bit 6, is OVER FLOW flag for timer 1; referred as TF1. When the 16 bit counter starts counting from zero, i.e. 0000H, it will go to 0001H, 0002H, so on till it reaches FFFFH. And thereafter to 0000H.

When timer rolls from all 1s(ie. FFFFH) to 0, this TF1 bit will set to bit "1"

2. Similarly bit 5 is, an OVER FLOW flag for timer 0 called (TF0) And is set to "1" when T0 rolls from all 1's to 0

3. Bit 6, is a control to enable the timer to count.(TR1). When changed by the programmer to bit "1" the counter T1 start to

count and when changed by the programmer to “0” it halts; but does not reset timer.

4. Similarly bit 5 is Start/Halt control for T0 timer. (TR0).

TCON SFR is a register Bit addressable register and has the bit representation as TCON.0 ,TCON1, ... to TCON.7.

The Programmer can change any one bit at a time, like reset the flag TF1 to “0” .

Timer Counter Interrupts.

The counters have been included on the chip to relieve the processor of timing and counting tasks. When the program wishes to count a certain number of internal pulses or external events, a number is placed in one of the counters.

The number represents the maximum count *less* the desired count, *plus* 1. The counter increments from the initial number to the maximum and then rolls over to 0000, on the final pulse and also sets a timer flag. The flag condition may be tested by an instruction to tell the program that the count has been accomplished, or the flag may be used to interrupt the program.

For example:

if I want to count 3 pulses or events, I will place $(256-3)+1 = 254$ as a number in a 8 bit counter mode. The counter will increment from 254 i.e. 255, 256, and then 0 & after these 3 counts the timer

flag will set. This flag will then be used by the CPU to go for the desired activity which is to be performed after 3 counts.

Timing operation

If a counter is programmed to be a timer, it will count the internal clock frequency of the 8051 oscillator divided by 12.

As an example, if the crystal frequency is 6.0 megahertz, then the timer clock will have a frequency of 500 kilohertz.

In order to reach these oscillator clock pulses to the timer, the C/T bit in the TMOD register must be set to 0 (timer operation). Bit TRX in the TCON register must be set to "1" (timer run), and the gate bit in the TMOD register must be "0", In other words, the counter is configured as a timer,

Timer Modes of Operation

The timers may operate in any one of four modes that are determined by the mode bits, M1 and M0, in the TMOD register.

The table 1, shown the four timer modes.

1) Timer Mode 0 (13 bit counter)

Setting the timer mode bits to 00b (binary) in the TMOD register results in using the upper register (THX i.e. TH1 OR TH0) as an 8-bit counter and TLX as a 5-bit counter; sets the timer 1 OR timer 0 as 13 bit counter.

As an example, the 6 megahertz oscillator frequency would result in a final frequency to TH of 15,625 hertz. The Timer flag is set whenever THX register goes from FFh to 00h, in 0.0164 seconds for a 6 megahertz crystal.

2) Timer Mode 1 (16 bit counter)

Mode 1 is similar to mode 0 except TLX register is configured as a full 8-bit counter instead of 5 bit; i.e. when the mode bits are set to 01b in TMOD SFR register.

3) Timer Mode 2 (8 bit Auto-Reload)

Setting the mode bits to 10b in TMOD register, configures timer to use only the (TLX) lower register counter as an 8-bit counter. While upper THX is used to hold a value that is loaded into TLX lower register, every time the lower timer register TLX overflows from FFh to 00h.

The Timer flag is also set when TLX overflows.

This mode exhibits an auto-reload feature. The lower count register TLX will count up from the number in THX; overflow, and then initialized again with the contents of THX.

For example, placing 9Ch in THX will result in a delay of exactly 0.0002 seconds before the Overflow flag is set, if a 6 megahertz crystal is used.

4) Timer Mode 3

In mode 0, 1, & 2, timer T1 & T0 operate independent of each other whereas, in mode3, the timer T1 & T0 operate with each other's configuration; so the understanding of this operation requires more practical exposure of 8051 working. Hence, I move to the next topic.

Counters

The only difference between counting and timing is the source of the clock pulses to the counters. When used as a timer, the clock pulses are sourced from the oscillator through the divide-by-12 circuit.

When used as a counter, pin T0 (Port P3.4) supplies pulses to counter 0, and pin T1 (P3.5) to counter 1.

The C/T bit in TMOD must be set to 1 to enable pulses from the TX (P3.4 OR P3.5) pin to reach the control circuit.

These are the reference /books, used for this module.

Thank you very much.