Welcome students to the paper liner

and digital integrated circuits

so it's 5 semester 3 paper.

In this module we will be learning about

the synchronous or the ripple counter.

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so the outline is as follows.

We will be looking at the asynchronous

counter so the learning outcomes

the student will be will be able to

understand and implement a counter.

So basically a counter is a device

which can count any particular

event on the basis of how many times

the particular event has occurred.

So in additional system one can.

This counter can count and store

the number of time any particular

event or process has occurred

depending on a clock signal.

So most common type of counter

is a sequential effect.

We call it a sequential digital

logic circuit with a single

clock input and multiple outputs.

So the outputs represent binary

or binary coded decimal numbers.

Each clock pulse you can either

have a app counter so the clock the

increases the number decreases the number.

So today the asynchronous counter

with asynchronous.

In fact it's sent for absence

of synchronization.

That means there is synchronization

is not there.

So each of the flip flop are

getting different clocks,

so they're not getting the same clock.

So let us take before we look

at the asynchronous counter.

We need to look at revise effect.

We almost have seen this that

what is a T flip flop?

How we call it the toggle flip flop so

at Flip Flop will first look at the

excitation table of the T flip flop.

The symbol I think in fact Flip

Flop is nothing but a JK flip flop

which has we have tied both the

inputs of our G and K2 BCC so that

is how we can get a T flip flow.

So the D flip flop the tables

that followed again.

Whenever there is,

when both the presets are zero,

the active low signals that we

can't use that because both of

them try to do it together,

so we can't use that state

remaining whenever preset is 0.

Again,

output queue is going to be forced

to one whenever clear is 0,

output is going to be forced to 0,

so we are not going to use a precedent

clear for a signal starter for the

normal normal binary counter later on

we will see that the use of the clear.

And 2nd is OK whenever the

presenting clear is one that means

they're inactive and a clock.

So whenever there's a clock and it

is in fact a one on all the time.

So whenever a clock is there and it is one,

what do you happen whenever

there's 2 + 1 output is going to

toggle output is toggling toggle

means whenever his Q is zero,

and suppose Q bar right now is 1.

Q is going to become one and Q bar is

going to become zero,

so it's going to take at least.

Clocks are cycle.

It's going to toggle.

And in case if there is no clock

present and our team is still one.

And that gives in that case,

what even happened is that output

is going to retain its state,

so it will say it's a memory state.

So all this counter students will

say that will make the assumption

that we have not shown it.

I'm not shown it away,

but all T1T2 let us say

they are all tied to 114.

So for us for us counted any.

For this to work, as in this counter,

all the things that has to be continued to

one at all times have not shown you here,

but that is the assumption which

will go through.

So now whenever there is a clock pulse,

so first thing what is going to happen,

a clear is now clear 0.

So what you do is going to do it

is going to force the output of

all the three flip flops to 000 it

respective whether right now T not T1

and T2 both are all are tied to one.

Let us say but.

Override all whatever is present and

we are going to get 000 now our clear

is made one so all the players are all

the flow is 1 and we are clock arrives.

What do you happen?

You know it is getting the clock

direct clock so only the output of

the first flip flop is going to

toggle the second flip flop is right

now earlier do not have any clock.

The clock in fact all the three

flip flops which are the flocks.

They are positive edge flip flops,

edge triggered flip flops.

So whenever there's a positive

edge that means remember the

clock goes from zero to 1.

So right now.

You the first flip flop had got a

positive edge whereas if you see

the second and third the second and

third flip flop are getting the

clock from the previous flip flop.

So two is getting a clock from.

In fact the previous flow that is T1

and T1 is getting the clock from T not.

But again I'm repeating at not one

to all Type 2 VCC will all one will

go to the assumption and yeah So

what is gonna happen right now,

only first preflop I struggled the

2nd and the 3rd Flipper continued to remain.

You know,

and a clear is 1 now,

what is going in the next clock cycle now?

If you take a look students over

here right now.

Q Not this QO is going to act like a

clock to the second clip clock and Q1 is

going to the clock to the third floor.

So in the next clock cycle again the first

flip clock if I go to the next slide,

AQ naughty is going to become zero.

It has toggled again and now

our Q1 has become one. Why?

Because now the second flip flop has

got a clock on the first one because it

was zero and Q node was one previously.

So it went from zero to 1.

So that is why a second flip flop also

now toggled because it got a flop.

Number first flip flop,

then the next clock cycle.

Now take a look over here.

The third flip flop.

Now if you take a look at the

third flip flop it is.

There is a possibility now that

from the next logical we are.

This is become one one now.

So that means in the next cycle

this third flip flop also is getting

a clock from the previous one.

So if you take a look if I turn the

next slide now what has happened?

The first flip flop will continuously

change 010101 the second flip

flop will change every second.

Not so good.

So first 200, then 11, then 0011 and so on.

And the third flip clock will take 3 cycles,

so it will be first 000,

then 111 and so on South.

If you take a look again again first

floor again toggle now second it will

toggle toggle the third like 601.

This is 001.

Now this change in the third

clock cycle and so on.

This is going to be a repetitive thing.

So in fact this was nothing.

But if you take a look this was

a 3 bit down counter.

The admin will start from.

This is going to 11111.

Do all the one each time

you're decrementing by one,

and if you take a look at the state diagram,

we are going to get around 8 state,

so this is a 3 bit down counter

asynchronous down counter.

If you take a look at excitation

table it's very simple to remember if

you take a look over here whenever

a clear is zero it will clear all

the three outputs Q1 and Q2 next.

After that we'll make our clear one.

So what is going to happen now?

The output in the first will

just take a look at the table.

The output of the first flip flop that is Q,

not each.

We'll take a look for whenever it

is getting a positive edge trigger.

You can take a look at the table of Q,

not it is changing stage every clock cycle,

and we know clear is 11 and we

have said that all our T not T1

and all the TT1 and T2 are tied

two which that is assumption which

is not shown over there.

But this assumption and all three are

111. So if you take a look over

here QO is changing each cycle so

10101010 if you take a look at Q1

because it is waiting for Q the output

of QO is acting as a block of Q1.

What is going to happen is

it is not going to change?

Every cycle which is equal to change the

output every two cycles so you can see

11001100 and in fact the third

flip flop has it is in fact

going to change up to three.

Sorry it is going to change

up to four clock cycles,

so one it will be 1111 and after

that after four cycles it is going

to become 0000 and if you take a

look at this the output of this

table start from 111 then it goes

now very important is our MSB

is towards the right hand side.

Normally when we look at any number,

it is towards the,

so that is an important observation.

We need to know that make that AQ not

is this side MSB towards the right.

So while interpreting the answer,

we'll have to look from, right?

So if you take a look,

it is 111110 so it is

676101100 which is

4011301020011000 and then this repeats.

It's a repetitive process so very

important thing is we understand Q2

is a MSB due to the MSB so this is

the timing diagram of the counter.

So again the same thing.

What you are seeing in the truth table.

It's similar over here so if you see

whenever the clear is 0 all the three

outputs are 000 and whenever there is a

clock over here if you just take a look at.

New node for every workload cycle it

is toggling for 101010 and so on.

Now for Q1, if you see Q1 is

waiting for Q not because Q naughty

is acting like a clock for Q1.

So whenever there is a transition from

zero to 1 because it's positive waiting

for a positive figure, a Q1 is changing.

So here there's a first.

This is like clean clock for Q1 so this is

the first edge over so Q1 was zero initially.

Now it has become one.

Now it will continue to

remain one when it changes.

Whenever it is OK here there's a

transition from zero to one of Q not so.

Then again it will change.

1200 So then again, you will see

here there's another clock over here.

Then again, it will be one one,

and so on.

If you take a look at Q2Q2 first.

If you look at for Q2Q1 is

a law for Q2Q1 is a clock,

so whenever Q1 goes from zero to one,

Q2 is seen from again zero data stalker

and then if you see Q1 is there is

no positive edge coming from Q1.

There is a negative edge,

but that's doesn't make a difference.

Finally,

we see that here after 4 clock cycles,

Q1 becomes higher from zero.

It goes from zero to 1 so that time.

You 2 gets that positive edge and then

it changes the state and it becomes 000.

If you take a look at the states it's again

111110 so we have to look from the bottom,

so 101100 and so on till 000 and

then it's a repetitive process.

So we can also have a synchronous

counter that is app counter.

Only difference is instead of looking

at Q not Q1Q2 we'll just have to

look at we'll place output at Q bar

Q1 bar North Q2 bar as a compliment.

So if you just take a look.

Those three diagram you can slide

just the opposite first Table 00,

then 001010 and so on till 111 S.

If you take a look at these

two table same true table.

Only thing I've just written

this Q not by Q1 warrant Q2 bar.

So if you take a look let's take

a look at Q and Q1 or Q bar.

So both are going to be complemented.

So what two is there the first few?

But will be 10101010.

So generally if you take the

complement of Q1 it is Q1 bar.

You're going to get

10011001 and one.

So in the Q2 bar complement of it,

we're going to get over here.

This 000 and 111.

Now if you take a look at this side

where the truth table over here,

you can see that it starts from

O1Q1Q2Q2 bar, Q1 bar and QR code bar 000,

then 001010 and so on till 111.

So if you just.

This output and the complement of the

all the flip flops we are going to

get are we are going to get a 3 bit

up counter so the dagger is exactly the same.

Only thing we're going to take the

output at a U-1 and U2 respectively.

So again, this same feature in the top

diagram is nothing but down counter,

and if you just take the compliment of that,

if you take this look over here.

You're the

1110000011. This is the 100 and so on.

So finally, when this is 000,

this is going to be 111.

So up counter done bit of

very easy to implement.

You just have to if you want a down counter.

We'll look at Q2Q1 Q If you

wanted down counter we look at

Q2 were Q1 bar North not bar.

Now if we don't normally if

we take any counter suppose

if we take a four bit counter.

If we say a 3 bit counter we are going

to have around two raise to North

States so it's a four bit counter.

Going to have 16 states.

The three bit counter we're

going to have around each states.

So what if we don't want all the states?

So can we stop the number of states?

As we say?

I just want we need 10 states

that are from zero to 9 or we

want maybe just five state from

zero to four stage from zero to.

4531024 that is 012394.

So we own five states.

So what is it possible? Yes.

So what we do we call such type

of controls that in fact we

call it as a truncated counter.

So normally if we don't truncate it

like for example so 4 bit counter see

the states of the counter students.

We also call it a mod or we

call it as modulus of a counter.

So the previous one what we saw

there were eight states over there.

So we can say it was a we can

call it a Mod 8 counter.

So if you don't want all the eight

states we want to stop it then we can.

Depending on many states you want,

suppose we want just five states,

so we'll call it a modify counter.

If you want only 10 states,

we'll call it a mod 10 counter.

So in fact this is called as a truncated asynchronous truncated counter.

Now how we do it if you don't truncate it,

we call it as a full sequence counter.

If we truncate it,

we call it as a signal strength counter.

Now how do we truncate it so we can

drink it is by using making use of

up reset or the clear we see which

one we're going to use and we're

going to use one of our gates gates,

which are always.

You earlier.

So if you take a look at this,

it's a mod Phi counter.

Same circuit, only thing now will take

the clear of all the three flip flops.

Again T not T1 and T2.

Remember we have said we have Type 2 VCC

and we give a clock over here and again.

Now this is going to work early as the

same in the same way and we're taking.

So this is the average.

We're taking output Q1Q2 bar,

so we know that you want to

work as up counter.

So what is going to happen?

The output of this Q naughty.

The one and two two bar.

They're all connected to.

They are connected to this nanger doyer.

And only if you take a look over,

it's already gonna happen.

I'll just go through the table over here.

So in this modified contour we are going

to have five stated formula 1243 and four.

So mod 5 min 5 states.

Now at this directly taken the output

is all the three flip flops here,

so we know that.

So what is going to happen

000001010011100? Now, whenever this

asynchronous counter reaches 101,

let us take a look at this clip and gate.

So Q naughty will be one.

Q1 bar will be 0 and Q2 bar will be also one.

When it is 1:01.

So the second flip flop is 0.

So we have put a nod curatorial.

The reason we want to make that also one.

So now if we make that one the zero of that.

So the 1:01 if you make that 0 to one.

So that means all the three inputs now

to the Nagata 111 and we know that.

And then good,

it is just the complement of an good.

So a NAND gate.

In fact, an gate where all the

inputs of an and gate are one that

is all the input have to be 1.

Then only the output is going

to be true or one.

So NAND gate is just the opposite.

So whenever all the inputs are

one that time all that time,

the output of the NAND gate

is definitely going to be 0.

So so whenever it becomes 101,

this output of this NAND gate is

definitely going to become zero

only for that condition remaining

all the other conditions.

In fact.

In fact, the NAND gate for remaining.

There's always output is 1,

so at that time the clear will be

inactive only for this particular state.

What is going to happen when it is 101,

just one output?

This NAND gate will become zero

and it is going to go to the clear

of all the flow 3 flip flops.

So if all the three levels are going

to get 00 student, what do you?

What happen all the time?

'cause will reset back to 000 and again

it will start the count from 001234 again.

It will become five again.

The output of the NAND gate is

going to become zero and the all

the three flip plug we get clear.

But if you take a look over here,

once you're ready for that 101,

you may just see it as a small glitch,

or you may not see that one.

So from 100 directly it has come back to 000,

then 001 and this will

be a repetitive process.

So this is the timing diagram similar

to what you have seen earlier.

If you take a look at this Q is

0011010011 and then back to

001100 and then back to zero.

So five states in total.

So these are references Thomas

Flight by digital fundamental Psi

Region Asia and. Things wouldn't.