

Unit 1

Module: Low power design: Power Consumption characteristics, Low Power modes

Introduction to Low power design

The various embedded applications and products have requirements of ultralow power MCUs. These devices are usually powered by a battery source and are currently achieving more than 10 years operation from a single button cell battery. So, there is a necessity for minimum power consumption. The battery capacity is limited; so, to make device run for a long time, it is required to have a low power microcontroller to design similar embedded systems. One of the salient features of the MSP430 is its very low power consumption.

Examples:

The various embedded applications and products like access control & security systems, electronic locks, electric meters, water meters, fitness and activity trackers, pulse oximeter, etc

Power/Current Consumption

- Current increases with clock frequency, roughly linearly.
- Current increases with supply voltage.
- More active peripherals means more current consumption, but a Timer unit running at 8 MHz draws considerably less current than the CPU running at 8 MHz

MSP430 works on two types of mode:

- 1) Active Mode
- 2) Low Power Modes (Standby Mode)

The MSP430 microcontroller is designed for ultralow-power applications. It offers the lowest power consumption and the perfect mix of integrated peripherals for a variety of battery-operated applications. MSP430 microcontroller has Low power modes (LPM) 0, 1, 2, 3, 4, and 3.5 and 4.5. AM is the normal running mode and all LPM for low power consideration modes. The low power operating modes consider the needs of ultralow-power consumption, speed, data throughput and minimization of individual peripheral current consumption.

LOW POWER MODES OF MSP430

- Active mode: CPU, all clocks, and enabled modules are active, $I \approx 300\mu A$. The MSP430 starts up in this mode, which must be used when the CPU is required.
- LPM0: CPU and MCLK are disabled, SMCLK and ACLK remain active, $I \approx 85\mu A$. This is used when the CPU is not required but some modules require a fast clock from SMCLK and the DCO.
- LPM1: Both CPU and MCLK are disabled. DCO(digitally controlled oscillator) is disabled. SMCLK is not available if it is sourced from DCO. ACLK remains active.
- LPM2: CPU, MCLK, SMCLK and DCO are disabled, ACLK remains active

- LPM3: CPU, MCLK, SMCLK, and DCO are disabled; only ACLK remains active; $I \approx 1\mu A$. This is the standard low-power mode when the device must wake itself at regular intervals and therefore needs a (slow) clock. It is also required if the MSP430 must maintain a real-time clock.
- LPM4: CPU and all clocks are disabled, $I \approx 0.1\mu A$. The device can be wakened only by an external signal. This is also called RAM retention mode.

The table below shows which clocks are active and which are disabled in various low power modes.

	CPU	MCLK	DCO	SMCLK	ACLK
LPM0	Disable	Disable	Available	Available	Available
LPM1	Disable	Disable	Disable	Available	Available
LPM2	Disable	Disable	Disable	Disable	Available
LPM3	Disable	Disable	Disable	Disable	Available
LPM4	Disable	Disable	Disable	Disable	Disable

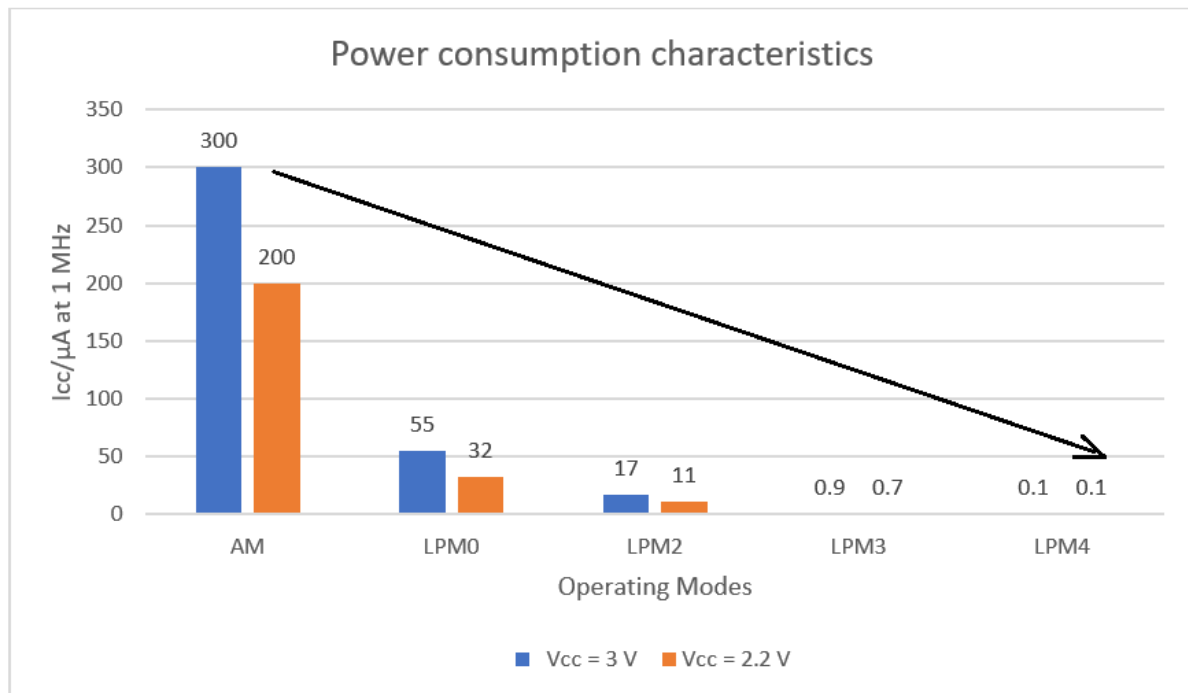
BITS of STATUS REGISTER and LOW POWER MODES

Four bits SCG1, SCG0, OSCOFF, CPUOFF are used to switch MSP430 from active mode to LPM. Values of bits according to modes are shown in the following table.

SCG1	SCG0	OSCOFF	CPUOFF	MODE	CPU and CLOCKS STATUS
0	0	0	0	Active	CPU is active, all enabled clocks are active.
0	0	0	1	LPM0	CPU, MCLK are disabled, SMCLK, ACLK are active.
0	1	0	1	LPM1	CPU, MCLK are disabled, DCO and DC generator are disabled if the DCO is not used for SMCLK, ACLK is active.
1	0	0	1	LPM2	CPU, MCLK, SMCLK, DCO are disabled, DC generator remains enabled, ACLK is active.
1	1	0	1	LPM3	CPU, MCLK, SMCLK, DCO are disabled, DC generator disabled, ACLK is active.
1	1	1	1	LPM4	CPU and all Clocks disabled.

Power consumption in various modes

Power consumption in various modes is shown in the following figure



C compiler instructions to enter into power down modes

Enter LPMx	C Compiler Intrinsic	Writing to SR with intrinsic
LPM0	<code>_low_power_mode_0();</code>	<code>_bits_SR_register(GIE+LPM0_bits);</code>
LPM1	<code>_low_power_mode_1();</code>	<code>_bits_SR_register(GIE+LPM1_bits);</code>
LPM2	<code>_low_power_mode_2();</code>	<code>_bits_SR_register(GIE+LPM2_bits);</code>
LPM3	<code>_low_power_mode_3();</code>	<code>_bits_SR_register(GIE+LPM3_bits);</code>
LPM4	<code>_low_power_mode_4();</code>	<code>_bits_SR_register(GIE+LPM4_bits);</code>