Quadrant **II – Transcript and Related Materials**

Programme: Bachelor of Science (Second Year)

Subject: Physics

Course Code: PYC 103

Course Title: Electronics

Unit: 20 C-E amplifier: Class A

Module Name: Graphical Analysis, Effect of adding A.C. load, Input and Output resistance.

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Notes:

C-E amplifier: Class A
Graphical analysis, Effect of adding A.C. load, Input and Output resistance.

C-E amplifier: Class A

Amplifier is the electronic control device which amplifies the applied input (ac signal).

For the purpose of circuit analysis - we consider linear amplifier, biased in the active region, input signals are low enough so as to restrict the operation in the linear region and the frequencies of the ac input signals is such that the capacitances in the circuit can be neglected.

The amplifiers may be classified in different ways, we consider two such classification one is according to circuit arrangement or mode of operation (C-B amplifier, C-E amplifier and C-C amplifier) and the other according to the point of operation i.e. depending on dc biasing (Class A, Class B, Class C and Class AB).

The common emitter amplifier (C-E amplifier) is such an amplifier where the emitter terminal is common to input and output. The input signal is applied across the base and emitter terminals and the output is taken across the collector and emitter terminals. For common emitter the collector current is given by the relation $I_C = \beta I_B + I_{CEO}$

where β is current amplification factor in C-E mode and is the ratio of output collector current to the input base current. Since the leakage current I_{CEO} is very small $I_C = \beta I_B$

The C-E amplifier configuration is one of the most widely used transistor configuration for electronic circuit design (amplifiers -audio amplifiers, analog amplifiers, in oscillators, basic switch etc.). C-E amplifier offers many advantages, It provides a voltage gain, moderate current gain and high power gain, medium input and medium output impedance and it has a 180^{o} phase change across the circuit.
Among PNP and NPN type transistor NPN is more commonly used.

Class A amplifier is one in which the operating point and the input signal are such that the current in the output amplifier flows for the whole of the input cycle. It operates essentially at the midpoint of the linear portion of its characteristics. In class A amplifier, the active device conducts for the full cycle of input signal. Power is drawn from d.c. source for full cycle of input signal. Efficiency of class A amplifier is low, Maximum theoretical efficiency is 50%. The practical value may be about 25%.

All voltage amplifiers an audio frequency amplifiers using only one transistor are operated in class A. Figure 1. shows npn transistor in common emitter configuration. In a C-E amplifier the input current and the output voltage are taken as independent variables whereas the input voltage and output current are taken as dependent variables

We may write

$V_{BE} = f_1(V_{CE}, I_B)$ 1

$I_C = f_2(V_{CE}, I_B)$ 2

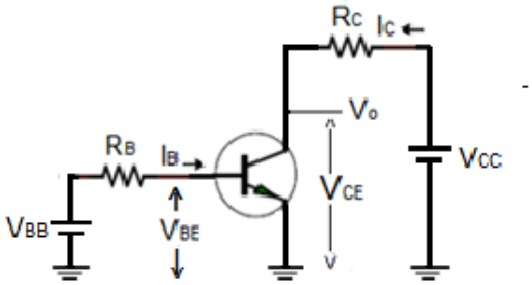

Figure 1. npn transistor in common emitter configuration.

Equation 1 describes the family of input characteristic curves, and equation 2 describes the family of output characteristic curves.

Typical input and output characteristic curves for a npn transistor are shown in Figure 2 and Figure 3. In Figure 3. the abscissa is the V_{CE} and the ordinate is the collector current I_C and the curves are given for various values of base current I_B, For a fixed value of base current I_B the collector current is not very sensitive value of V_{CE}. The transistor is operated within limits of its operation

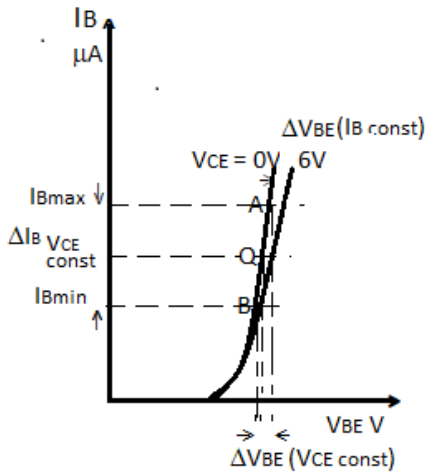

Figure 2. Typical CE amplifier Input characteristics npn transistor.

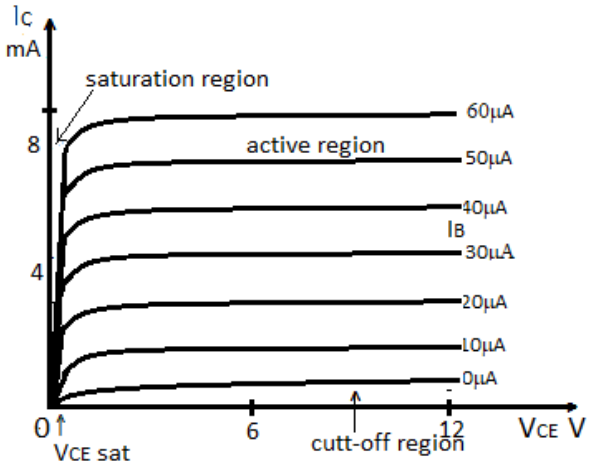

Figure 3. Typical CE amplifier Output characteristics npn transistor.

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Load lines and Operating point.

Biasing refers to the DC voltages applied to the transistor for it to turn on and operate in the forward active region, so that it can amplify the input AC signal.

One of the simplest transistor circuits is known as fixed-bias circuit. Figure 4. shows a fixed bias circuit. The circuit is biased by a single dc power supply, and the quiescent base current is fixed by the resistor R_B. The coupling capacitors C_C acts as an open circuit to dc, isolating the signal source from the base current, they confine dc quantities to the transistor and its bias circuitry.

Consider a fixed bias circuit as shown in the Figure 4.

Applying KVL to the output circuit we have

$V_{CC} = V_{CE} + i_C R_L$

$V_{CE} = V_{CC} - i_C R_L$

$i_C = (-1/R_L)V_{CE} + V_{CC}/R_L$

equation of the type y = - mx+c (st. line equation),

V_{CE} and I_C are variables.

Consider Two points are from this equation

1) $i_C = 0$ $V_{CE} = V_{CC}$ and 2) $V_{CE} = 0$ $i_C = V_{CC}/R_L$.

These two points say point A and B are marked on the output characteristic curves of the amplifier Figure 5.

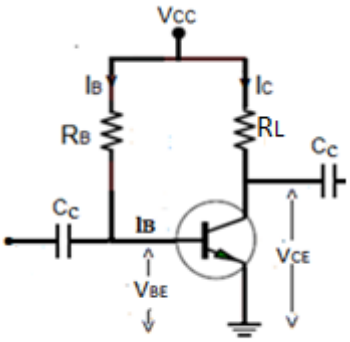

Figure 4. Fixed bias circuit.

The line joining these points is called static or dc load line. Thus the load line is the locus of all pairs of values of i_C and V_{CE} which can exist for a given value of V_{CC} and R_L, the load line depends on V_{CC} and R_L, it does not depend on the characteristics of the amplifier. The slope depends on R_L only.

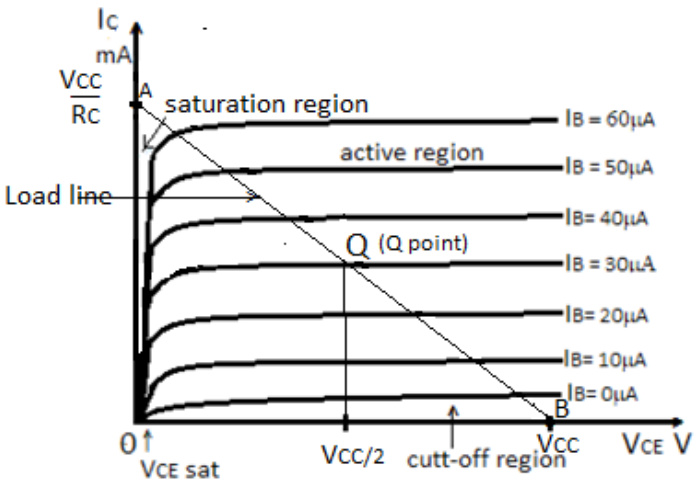

Figure 5. Class A operation of CE amplifier

The intersection of the load line with the output characteristic curves for a given base current is the operating point or quiescent point or Q point of the transistor amplifier. Thus the load line is a locus of all the sets of i_B, I_C, and V_{CE} that can exists for a particular transistor for a given V_{CC} and R_L. It is a locus of all possible operating points for the device for a given circuit.

Load line is very useful for the analysis of the performance of a transistor amplifier. The Q-point gives the required dc base current I_B, dc collector voltage V_{CE} and the dc collector current I_C in the active region of the transistor characteristics. The Q point is determined by finding the dc value of the base current I_B that will be supplied by V_{CC}, The equation for the input current

$V_{CC} = I_B R_B + V_{BE}$ (0.6v for Si) $I_B = V_{CC}/R_B$, The Q point is given by the interaction of the characteristic curve with for $I_B = V_{CC}/R_B$ with the dc load line.

For Class A amplifier V_{CE} voltage should be chosen midway the load line i.e. $V_{CC}/2$.

AC load line.

Every amplifier sees ac load along with dc load. The ac load may be found by the equivalent impedances of the circuit components in the emitter collector circuit. AC load lines (dynamic load lines) must pass through the Q point, because the collector current under static conditions remains unchanged. **(**operating point is chosen under zero input signal condition of the circuit). The effective ac load resistance Rac, is a combination of R_C parallel to R_L i.e. $R_{ac} = R_L \| R_C$. So the slope of the ac load line CQD will be (-1/Rac).

To draw the ac load line, two end points, i.e. V_{CE}(max) and I_C(max) when the signal is applied are required.

$V_{CE\,(max)} = V_{CEQ} + I_{CQ}R_{ac}$ (point D on the V_{CE} axis)

$I_{C(max)} = I_{CQ} + V_{CEQ}/Rac$ (point C on the I_C axis)

By joining points C and D, ac load line CD is constructed. As $R_C > Rac$, The dc load line is less steep than ac load line. Figure 6. shows Fixed bias circuit connected to external load R_L and Figure 7. shows output characteristics of CE class A operation of amplifier displaying both dc and ac load lines.

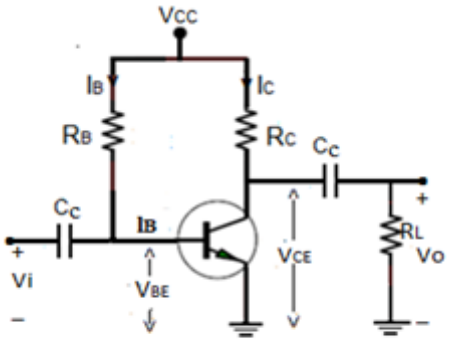

Figure 6. Fixed bias circuit connected to RL

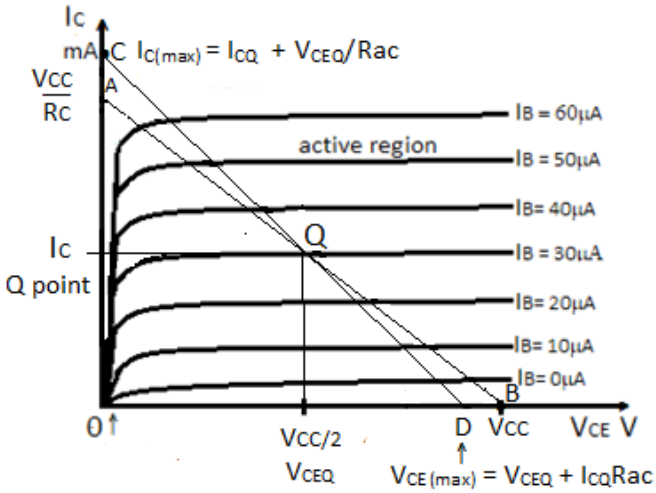

Figure 7. Class A operation of C-E amplifier showing dc and ac load lines.

Graphical Analysis.

The amplifier can be analysed for its performance by the graphical analysis. The current gain and voltage gain of an amplifier circuit may be obtained by using output characteristic of the transistor showing dc load line and the Q point for class A operation of transistor. When an ac input is applied, the variations of the instantaneous collector current and collector emitter voltage takes place along dc load line. It will swing the Q point up and down along the load line. When positive half-cycle of input base current is applied, the Q point shifts to point A'. Similarly, during negative half-cycle of input base current, Q point shifts to point B'. The input – output wave forms are shown in Figure 8. super imposed on output characteristics of CE amplifier.

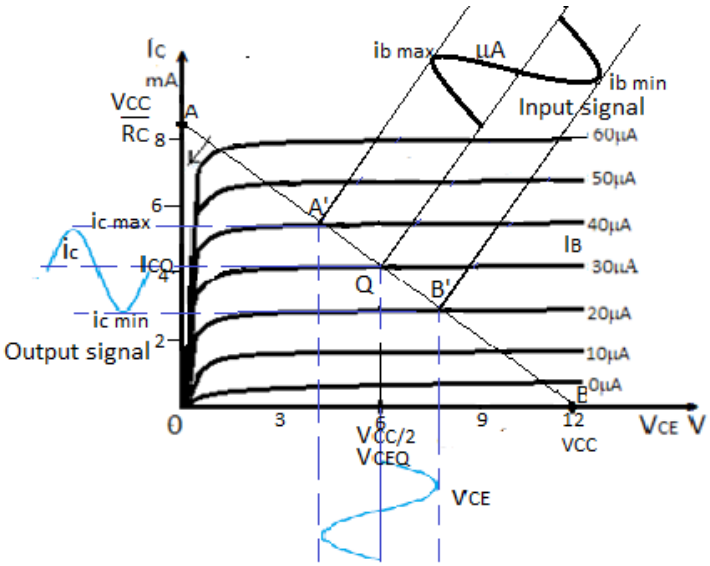

Figure 8. Class A operation of CE amplifier showing dc, ac load lines and input output waveforms

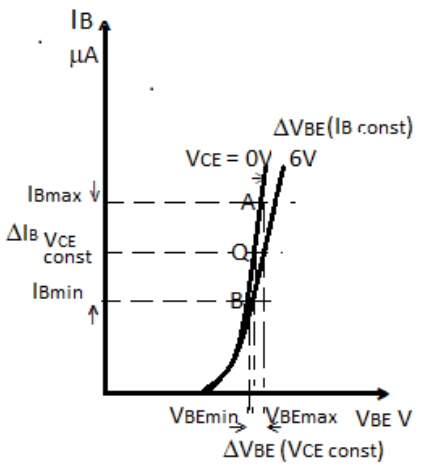

Figure 2. Typical CE amplifier Input characteristics npn transistor.

When input signal Vs (sinusoidal having v_{p-p}) is supplied, source current Is is given by some value i_{p-p} due to which V_{BE} will also undergo a change $v_{be\ p-p}$.

The base current will be driven from i_{bmax} to i_{bmin}

$i_{bmax} = I_B + i_p$ and $i_{bmin} = I_B - i_p$,

ac component of current is $i_{p-p} = i_{bmax} - i_{bmin}$

From the input characteristics, consider points AQB

At point A, i_{bmax} corresponds to v_{BEmax},

at point Q I_bQ corresponds to V_{BEQ}

at point B i_{bmin} corresponding to v_{BEmin}

Therefore base voltage varies from v_{BEmax} to v_{BEmin}

ac component of voltage $v_{bp-p} = v_{BEmax} - v_{BEmin}$

The corresponding collector voltages and collector current is obtained from dc load line.

At point A' (i_{Cmax}, v_{CEmin}), at point Q (I_{CQ}, $V_{CE}=V_{CC}/2$) and at point B' (i_{Cmin}, v_{CEmin})

ac component of collector current through R_C is $i_{Cmax} - i_{Cmin} = i_{cp-p}$

ac component of voltage across collector – emitter ($v_{CEmax} - v_{CEmin}$) = v_{CEp-p}

Current Gain Ai.

It is defined as the ratio of change in the output collector current to corresponding change in the input base current keeping the output collector voltage constant.

$= (i_{Cmax} - i_{Cmin}) / i_{p-p} = i_{cp-p} / i_{bp-p} \quad | V_{CE}$

$= \Delta I_C / \Delta I_B \; | V_{CE}$

Voltage Gain Av.

It is defined as the ratio of change in the output collector voltage to corresponding change in the input base current with the keeping the input base current constant.

$(v_{CEmax} - v_{CEmin}) / (v_{BEmax} - v_{BEmin}) = v_{CEp-p} / v_{bp-p} \quad | I_B$

$\Delta V_{CE} / \Delta V_{BE} \quad | I_B$

Power gain Ap = Av x Ai

As C-E mode has voltage gain as well as current gain , Power gain is much higher than in C-B mode.

Effect of adding Load line.

When we consider ac load R_L, The effective ac load resistance Rac, is a combination of R_C parallel to R_L . Slope of the **ac load line** CQD will be (-1/Rac) Being parallel Rac is smaller than smallest.

When variation in the base current takes place, the swing in collector current and collector voltage must be along ac load line representing an ac load resistance Rac instead of R_C with a slope (-1/Rac) ampere per volt. Since the voltage is more steeper than earlier, Voltage gain reduces. Since output characteristics curves are almost horizontal, the current gain is practically unaffected (increases by very small amount).

Power gain reduces because voltage gain reduces.

Input and Output resistance.

The dc/ac input and output resistance of the transistor can be found from the input and output characteristics curves Figure 2. And Figure 3.

DC Input resistance.

From the figure dc input resistance $R_{in} = V_B/I_B$,

Input resistance.

It is defined as the ratio of the change in input base voltage to the change in input base current with the output collector voltage V_{CE} kept constant.
$\Delta V_{BE}/\Delta I_B \mid V_{CE}$

It is the reciprocal of slope of CE input characteristics I_B versus V_{BE} keeping V_{CE} constant

Output resistance.

It is defined as the ratio of change in the output collector voltage to corresponding change in the output collector current with the input base current I_B kept constant. $\Delta V_{CE}/\Delta I_C \mid I_{B.}$