Quadrant II – Transcript and Related Materials

Programme: T.Y.B.Sc.

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Paper Title: Analog and Digital Electronics – Section I

Unit 5: Timers

Module Name: Astable and Voltage Controlled Oscillator (VCO)

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Notes

Astable multivibrator using IC 555:

- When the flip-flop output Q is low, the transistor T remain cut off and the capacitor C starts charging through R_A and R_B with charging time constant $[(R_A+R_B)C]$. The capacitor charges exponentially.
- As the capacitor charges, the voltage across the capacitor increases and when it reaches to $2/3V_{CC}$ and becomes slightly greater than $2/3V_{CC}$, the output of upper comparator goes high and it sets the flip-flop with Q high. Hence, transistor T saturates and its collector voltage drops to approximately 0V.
- Now, the capacitor C starts discharging through R_B only with discharging time constant (R_BC). When the capacitor voltage drops slightly below $1/3V_{CC}$, the output of lower comparator goes high again and resets the flip-flop thereby generating a rectangular pulse at the output.
- To avoid accidental reset of the flip-flop inside the timer IC 555, pin4 (reset terminal) is connected to V_{CC}. A bypass capacitor of 0.01µf is connected between pin5 (control voltage terminal) and ground.
- If $R_A << R_B$ than the duty cycle of the output wave approaches 50% which represents a symmetrical square wave. Duty cycle can also be made 50% by connecting a diode across R_B and keeping $R_A \approx R_B$.

Voltage controlled oscillator using IC 555:

- In a Voltage controlled oscillator which is also called Voltage to frequency converter, a control voltage (V_C) is applied to the control voltage terminal (pin5) of timer IC 555. This voltage not only modify the duty cycle but also affects the period and frequency of output waveform. The frequency depends linearly on the control voltage V_C applied and that is why it is called voltage controlled oscillator or voltage to frequency converter.
- In timer IC 555 pin5 is connected to inverting input of upper comparator. Normally, control voltage is $2/3V_{CC}$ because of internal voltage divider network. However, when voltage from external potentiometer is applied, the control voltage is given by

  $$V_C = \frac{R_1}{(R_1+R_2)} . V_{CC}$$

- When control voltage (V_C) is applied, the voltage across the capacitor varies between $1/2V_C$ to V_C instead of $1/3V_{CC}$ to $2/3V_{CC}$. If we increase the value V_C it takes the capacitor longer time to charge and discharge thereby changing the frequency.
- When the flip-flop output Q is low, the transistor T remain cut off and the capacitor C starts charging through R_A and R_B exponentially.
- As the capacitor charges, the voltage across the capacitor increases and when it reaches to V_C and becomes slightly greater than V_C, the output of upper comparator goes high and it sets the flip-flop with Q high. Hence, transistor T saturates and its collector voltage drops to approximately 0V.
- Now, the capacitor C starts discharging through R_B only. When the capacitor voltage drops slightly below $1/2V_C$, the output of lower comparator goes high again and resets the flip-flop thereby generating a rectangular pulse at the output.
